REMARKS

Claims 1-5, 16-21, and 23 are currently pending. Claims 6-15, 22, and 24-27 were previously withdrawn. Claims 1-3, 16, 18 and 19 have been amended. No new matter has been added. Applicants reserve the right to pursue original and other claims in this and in other applications.

Claim 1 stands objected to due to formalities as the Patent Office suggests that there is "no spaces between words" in lines 21-22. Applicants has reviewed the published patent application that corresponds to the instant case and has confirmed that these lines of claim 1 as reflected in the specification are properly reflected in the associated patent application. As such the objection is moot and should be withdrawn.

Claim 1 and 16 stand rejected under nonstatutory double patenting as being obvious over claims 1 and 4 of U.S. Patent No. 6,406,990 (" '990"). The Patent office suggest that claims 1 and 4 of '990 have all of the limitations of claims 1 and 16 of the instant application. Applicants respectfully traverse this rejection.

Claim 1 of the '990 patent recites, *inter alia*, "A method of mounting a semiconductor chip on a circuit board, said semiconductor chip having a terminal bump, said circuit board having a wiring pattern with an electrode area and a thermoplastic resin coat covering the electrode area of the wiring pattern, said method comprising the steps of:
heating and melting the thermoplastic resin coat of said circuit board; pressing the terminal bump of said semiconductor chip on the thus melted thermoplastic resin coat while applying an ultrasonic wave to the terminal bump so that the terminal bump penetrates the melted thermoplastic resin coat and comes into contact with the electrode area; bonding the terminal bump and the electrode area by continuously applying an ultrasonic wave to the terminal bump while in contact with the electrode

area; and cooling and solidifying the melted thermoplastic resin coat so as to securely mount said semiconductor chip on said circuit board."

Claim 1 of the instant application recites, *inter alia*, "A method for manufacturing an electronic component module having a semiconductor bear chip packaged on a wiring board, said method including: preparing said wiring board including a wiring pattern, a thermosetting resin film covering an electrode area on said wiring pattern and having insulating particles dispersed and included, and a thermoplastic resin film covering said thermosetting resin film; pressing a bump of the semiconductor bear chip onto the thermoplastic resin film in a melted state where said thermoplastic resin film is heated and softened, while applying an ultrasonic wave, so that the melted thermoplastic resin film is shoved away by said bump of the semiconductor bear chip and that said bump reaches a surface of said thermosetting resin film; pressing said bump against said thermosetting resin film by continually applying said ultrasonic wave to said bump so that said insulating particles are separated from within the thermosetting resin film, the thermosetting resin film is shaved away by said bump, and said bump makes contact with said electrode area; ultrasonically bonding said bump and said electrode area by continually applying said ultrasonic wave in a state where said bump and said electrode area are contacted; and bonding a semiconductor bear chip main body on said wiring board by cooling and solidifying said melted thermoplastic resin."

The '990 claimed invention is different from claimed invention in the instant application, in that the '990 claims fail to at least disclose the limitation of "a thermosetting resin film covering an electrode area on said wiring pattern and having insulating particles dispersed and included." The '990 claims also fail to disclose the limitation of "pressing said bump against said thermosetting resin film by continually applying ultrasonic wave to said bump so that said insulating particles are separated

from within the thermosetting resin film, the thermosetting resin film is shaved away by said bump, and said bump makes contact with said electrode area." Furthermore, the '990 patent is a U.S. patent that has a corresponding foreign counterpart, Kawai EP 1 104 017 (" '017"), which is also discussed below. Commenting on the '017, the Examiner confirms that the '017 "fails to disclose the formation of a thermosetting resin film."

Thus the subject matter of claim 1 of the instant application is not rendered obvious from claims of the '990 patent. The rejection of claim 1 should be withdrawn and the claim allowed.

Claim 16 has similar limitations as claim 1 and is not rendered obvious from the claims of the '990 patent.

Claims 1-5, 16-21, and claim 23 stand rejected under 35. U.S.C. 103(a) as being unpatentable over Kawai '017 in view of Kajiwara et al (EP 1 205 970)("Kajiwara")

The '017 reference discloses: "To provide a semiconductor chip mounting method by a flip-chip connection method in which a semiconductor chip can be mounted on a circuit board promptly, electrically and mechanically surely and further at a low cost, a process for pushing a melted thermoplastic resin coat aside by pressing a bump of the bare semiconductor chip on the melted thermoplastic resin coat applying an ultrasonic wave in a state in which the thermoplastic resin coat covering an electrode area on a wiring pattern is heated and melted and touching the bump and the electrode area, a process for bonding the bump and the electrode area by continuously applying an ultrasonic wave in a state in which the bump and the electrode area are touched and a process for cooling and solidifying the melted thermoplastic resin coat and bonding

the body of the bare semiconductor chip on the circuit board are provided." (Kawai, abstract).

The '017 reference at least fails to disclose the limitation of "a thermosetting resin film covering an electrode area on said wiring pattern and having insulating particles dispersed and included." Nor does the '017 reference disclose the limitation of "pressing said bump against said thermosetting resin film by continually applying ultrasonic wave to said bump so that said insulating particles are separated from within the thermosetting resin film, the thermosetting resin film is shaved away by said bump, and said bump makes contact with said electrode area." Nor does the '017 disclose "a thermoplastic resin film covering said thermosetting resin film." Furthermore, the Examiner confirms that the '017 "fails to disclose the formation of a thermosetting resin film."

Kajiwara fails to address the deficiencies of the '017 reference. Kajiwara discloses "A semiconductor device includes a semiconductor chip (1) and a printed circuit board (4). Metal electrodes (2) of the semiconductor chip (1) and the internal connection terminals (5) of the printed circuit board (4) are electrically connected through the metallic joining via precious metal bumps (3). A melting point of a metal material constituting each of the metallic joining parts is equal to or higher than 275 degrees, and a space defined between the chip and the board is filled with resin .... Containing 50 vol% or more inorganic fillers." (Kajiwara, abstract)

At the very least, Kajiwara fails to disclose both a " thermoplastic resin film" and a "thermosetting resin film," thus fails to disclose "a thermoplastic resin film covering said thermosetting resin film." As such, the rejection of claim 1 should be withdrawn and the claim allowed.

Claims 2-5 depend, directly or indirectly, from claim 1 and are allowable for at least the reasons noted above with respect to claim 1.

Claim 16 has similar limitations as claim 1 and is allowable for at least the same reason as claim 1.

Claims 17-21 and 23 depend, directly or indirectly, from claim 16 and are allowable for at least the reasons noted above with respect to claim 16.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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